APPLICATION NOTE

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APPLICATION NOTE
Design & Installation of High Speed Micro-D PCB Connectors

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REVISION HISTORY

REVISION	DATE	REVISED PAGES	REVISIONS
A	4/10/20		Initial Release
B	7/22/22		Added Section 4.3 per DCN 92407
C	9/15/23	6-8	Modified Section 4.1 and added 4.3.2 per DCN 97474
D	8/5/2024	8	Modified Section 4.3.2 per DCN 97474 per DCN101608

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1.0 Purpose

This document describes the proper way to design PCBs for the installation of PC tail and surface mount leads found on High Speed Micro-D connectors.

2.0 Referenced Documents

Document Number/Name	Description
GHSM-BSS	High Speed Micro-D Straight Surface Mount PCB Connectors
GHSM-HBR	High Speed Micro-D Hybrid Right Angle PCB Connectors
GHSM-1003	High Speed Micro-D Straight Surface Mount PCB Layouts
GHSM-1004	High Speed Micro-D Hybrid Right Angle PCB Layouts
GHSM-1002	Arrangements, High Speed Micro D

Table 1. Reference Documents

3.0 Responsibility

This document is the responsibility of the Engineering team.

4.0 Methods of Performance Optimization

4.1 Straight PC Tails (Thru Hole)

4.1.1 PCB Design

To achieve optimal impedance matching at the PC tail/PCB transition, utilize layouts shown in GHSM-1004 with the additional manufacturing information shown below:

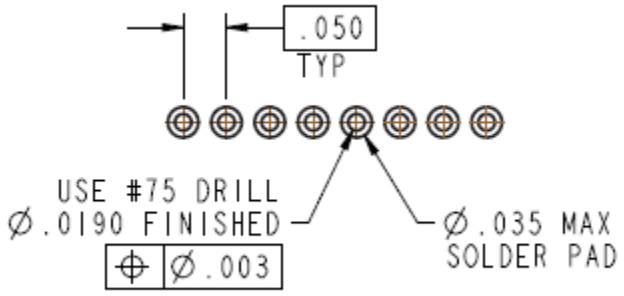

Figure 1 – Optimized PCB Layout for Thru Hole

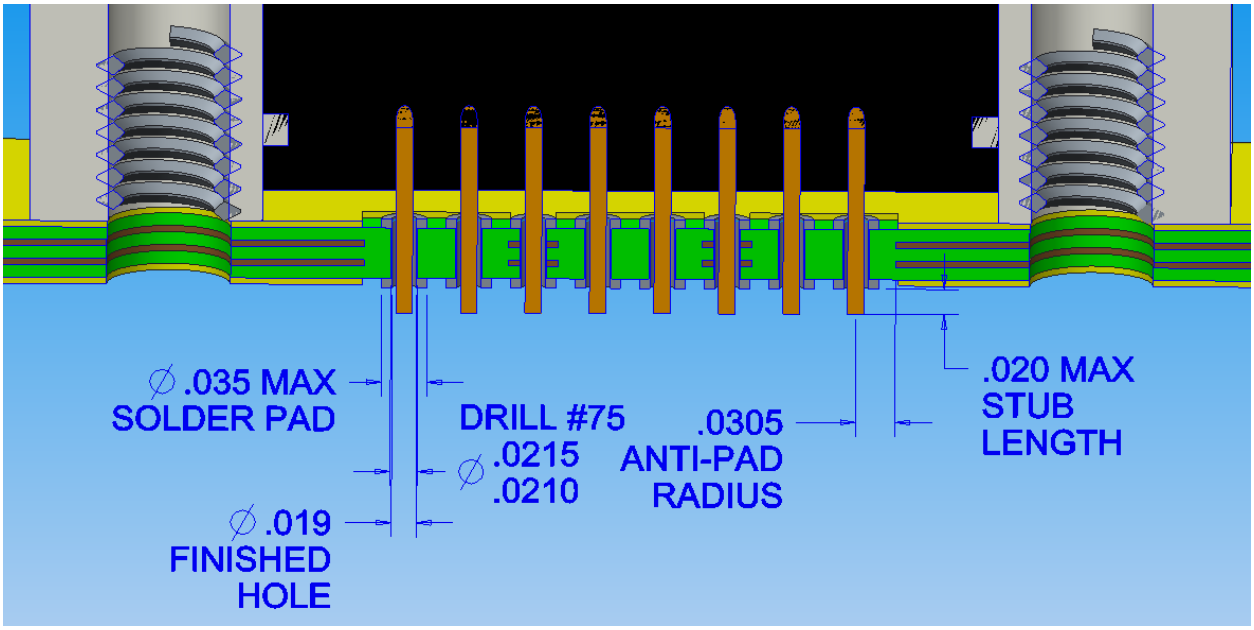

Figure 2 – Optimized PCB Cross Section for Thru Hole

4.1.2 IPC-A-610 Compliance

Thru hole design recommendations described by this document do not meet minimum annular ring thickness requirements of IPC-A-610 Class 3. Contact Glenair factory for more information.

4.1.3 Installation onto Board

To minimize the length of capacitive stubs, which lower impedance and cause the signal to resonate, we recommend trimming the PC tails to a length of .020 inches max per Figure 2.

4.1.4 Trace Routing

To reduce the effective length of capacitive stubs further, route the traces for the high-speed lines using PC tail terminations on the opposite side of the board from the connector.

Avoid right angles at trace to pad and other similar transitions throughout the signal path layout.

Signal trace widths and spacing are dependent on the desired impedance in addition to the PCB Stack-up, PCB materials, and routing traces as coupled or de-coupled. Reference Figure 3 for an example layout.

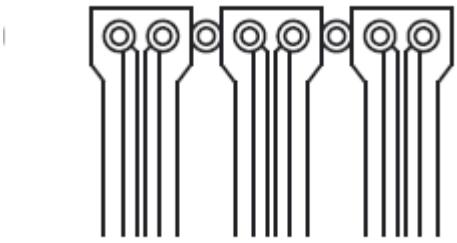

Figure 3 – Example PCB Thru Hole Layout, Termination Side

4.2 Surface Mount Leads

4.2.1 PCB Design

To achieve optimal impedance matching at the SMT lead/PCB transition, utilize layouts shown in GHSM-1003 and GHSM-1004.

4.2.2 Trace Routing

Like Thru Hole, SMT best practices include avoiding right angles at trace to pad and other similar transitions throughout the signal path layout.

SMT anti-pad geometry, in addition to signal trace widths and spacing, are dependent on the desired impedance in addition to the PCB Stack-up and PCB materials. Some applications will not require anti-pads. Reference Figure 4 for an example layout.

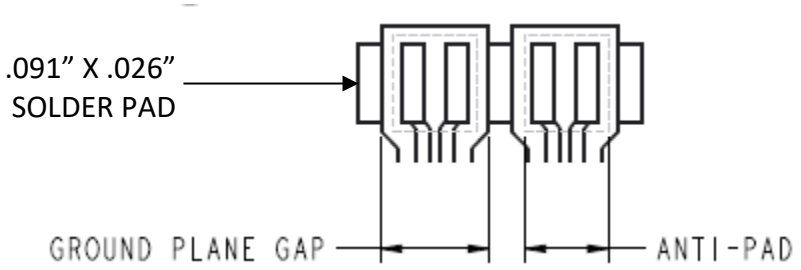

Figure 4 – Example PCB SMT Layout, Component Side

4.3 Hybrid Board Right Angle (Series GHSM-HBR and GHSRPM-HBR) Considerations

4.3.1 Escape Routing for Ethernet Applications

The hybrid connector incorporates routing aspects from both through hole and surface mount connectors. As with the through hole connector, routing should be performed on the opposite side of the board from the connector. This reduces the stub effect for PC tail terminations. For the surface mount pads, vias should be used to transition the signal to the layer opposite to the connector. The vias should be placed in the toe of the connector SMT pad to reduce the stub effect of the SMT pad. Figure 5 below depicts the via placement and escape routing for the recommended Ethernet pin assignments.

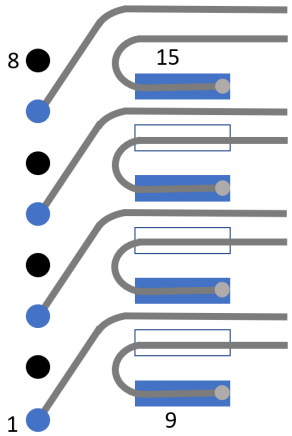

Figure 5 – Example PCB Hybrid Routing for Ethernet Applications

4.3.2 Skew Compensation

Due to connector geometry, the SMT tails are 0.164" longer than the PTH tails at the point where the tails meet the board. This corresponds to a ~26 ps longer propagation delay for the SMT tails. This intra-pair skew may have to be compensated, depending on the application.